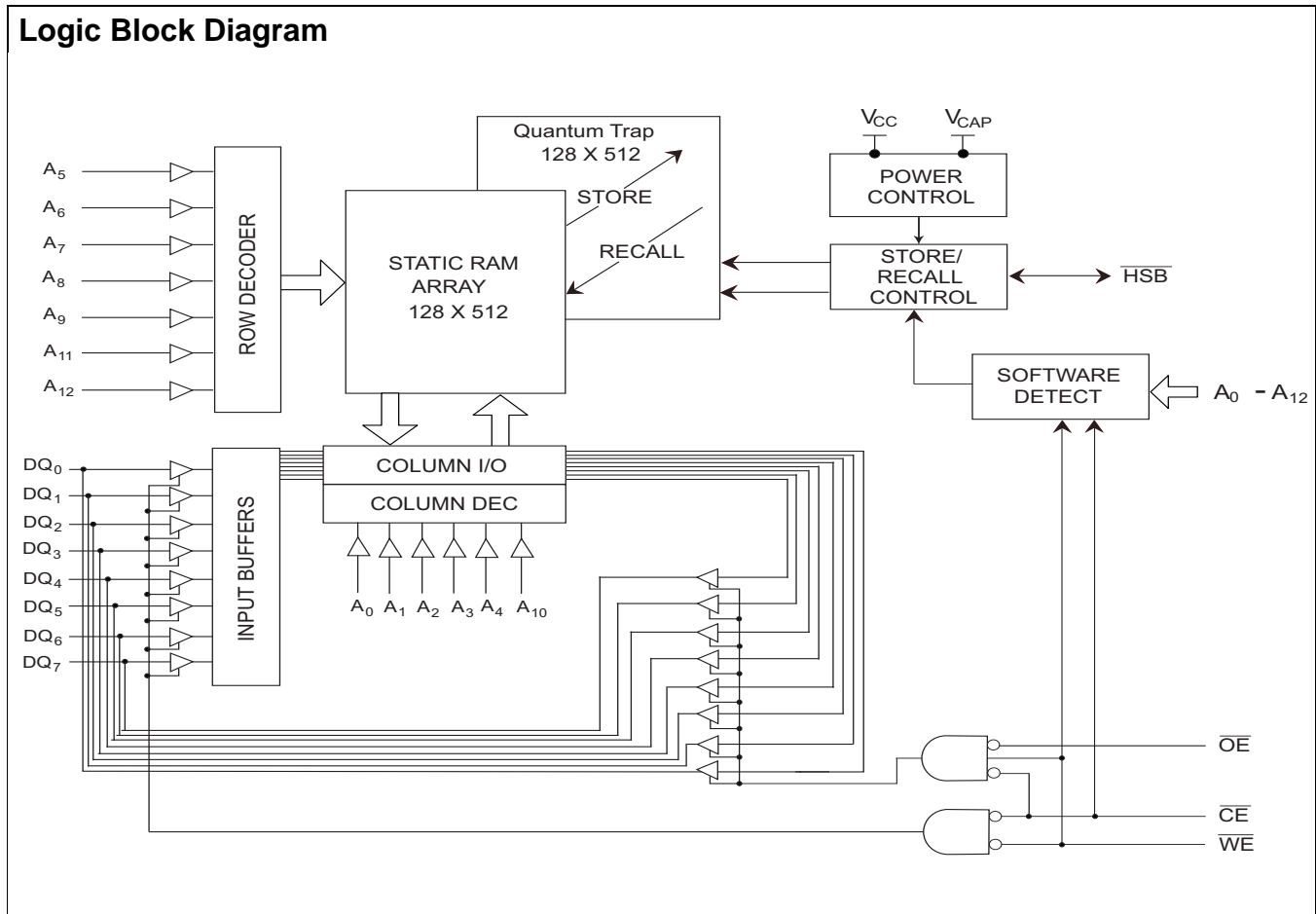


**Features**

- 25 ns and 45 ns access times
- Hands off automatic STORE on power down with external 68 mF capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Unlimited READ, WRITE and RECALL cycles
- 10 mA typical ICC at 200 ns cycle time
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5V operation +10%
- Commercial temperature
- SOIC package
- RoHS compliance

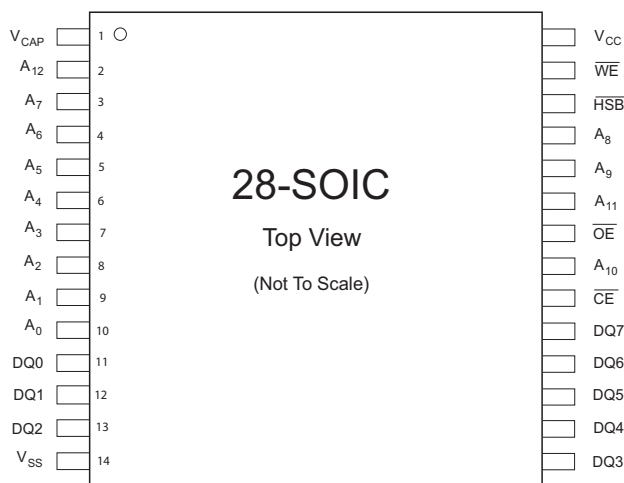
**Functional Description**

The Cypress CY14E064L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE is initiated with the HSB pin.



NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

## Pin Configurations



## Pin Definitions

Pin Name	IO Type	Description
A <sub>0</sub> -A <sub>12</sub>	Input	<b>Address Inputs.</b> Used to select one of the 8,192 bytes of the nvSRAM.
DQ0-DQ7	Input or Output	<b>Bidirectional Data IO lines.</b> Used as input or output lines depending on operation.
$\overline{WE}$	Input	<b>Write Enable Input, Active LOW.</b> When selected LOW, writes data on the IO pins to the address location latched by the falling edge of $\overline{CE}$ .
$\overline{CE}$	Input	<b>Chip Enable Input, Active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	<b>Output Enable, Active LOW.</b> The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
V <sub>SS</sub>	Ground	<b>Ground for the Device.</b> The device is connected to ground of the system.
V <sub>CC</sub>	Power Supply	<b>Power Supply Inputs to the Device.</b>
$\overline{HSB}$	Input or Output	<b>Hardware Store Busy (HSB).</b> When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V <sub>CAP</sub>	Power Supply	<b>AutoStore Capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.

## Device Operation

The CY14E064L nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14E064L supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

## SRAM Read

The CY14E064L performs a READ cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW while  $\overline{WE}$  and HSB are HIGH. The address specified on pins A<sub>0-12</sub> determines the 8,192 data bytes accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t<sub>AA</sub> (READ cycle 1). If the READ is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at t<sub>ACE</sub> or at t<sub>DOE</sub>, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t<sub>AA</sub> access time without the need for transitions on any control input pins, and remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or  $\overline{WE}$  or HSB is brought LOW.

## SRAM Write

A WRITE cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs are stable prior to entering the WRITE cycle and must remain stable until either  $\overline{CE}$  or  $\overline{WE}$  goes HIGH at the end of the cycle. The data on the common IO pins I/O<sub>0-7</sub> are written into the memory if it is valid t<sub>SD</sub>, before the end of a  $\overline{WE}$  controlled WRITE or before the end of an  $\overline{CE}$  controlled WRITE. Keep  $\overline{OE}$  HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If  $\overline{OE}$  is left LOW, internal circuitry turns off the output buffers t<sub>HZWE</sub> after  $\overline{WE}$  goes LOW.

## AutoStore Operation

The CY14E064L stores data to nvSRAM using one of three storage operations:

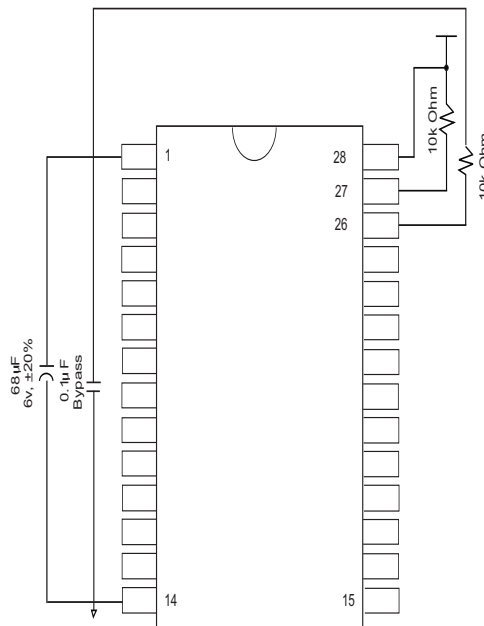
1. Hardware store activated by  $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E064L.

During normal operation, the device draws current from V<sub>CC</sub> to charge a capacitor connected to the V<sub>CAP</sub> pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V<sub>CC</sub> pin drops below V<sub>SWITCH</sub>, the part automatically disconnects the V<sub>CAP</sub> pin from V<sub>CC</sub>. A STORE operation is initiated with power provided by the V<sub>CAP</sub> capacitor.

Figure 1 shows the proper connection of the storage capacitor (V<sub>CAP</sub>) for automatic store operation. Refer to the DC Electrical Characteristics on page 7 for the size of V<sub>CAP</sub>. The voltage on the V<sub>CAP</sub> pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on  $\overline{WE}$  to hold it inactive during power up.

Figure 1. AutoStore Mode

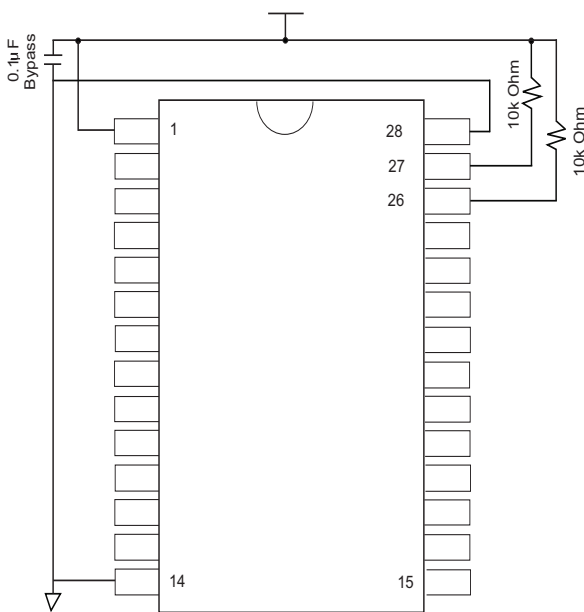


NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

In system power mode, both  $V_{CC}$  and  $V_{CAP}$  are connected to the +5V power supply without the 68  $\mu\text{F}$  capacitor. In this mode, the AutoStore function of the CY14E064L operates on the stored system charge as power goes down. The user must, however, guarantee that  $V_{CC}$  does not drop below 3.6V during the 10 ms STORE cycle.

If an automatic STORE on power loss is not required, then  $V_{CC}$  is tied to ground and + 5V is applied to  $V_{CAP}$  (Figure 2). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the CY14E064L is operated in this configuration, references to  $V_{CC}$  are changed to  $V_{CAP}$  throughout this data sheet. In this mode, STORE operations are triggered through software control or the HSB pin. It is not permissible to change between these three options at will. To reduce unnecessary

Figure 2. AutoStore Inhibit Mode



nonvolatile stores, AutoStore and Hardware Store operations are ignored, unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.

### Hardware STORE (HSB) Operation

The CY14E064L provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the STORE operations. The  $\overline{\text{HSB}}$  pin is used to request a hardware STORE cycle. When the  $\overline{\text{HSB}}$  pin is driven LOW, the CY14E064L conditionally initiates a STORE operation after  $t_{\text{DELAY}}$ . An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations, that are in progress when  $\overline{\text{HSB}}$  is driven LOW by any means, are given time to complete before the STORE operation is initiated. After  $\overline{\text{HSB}}$  goes LOW, the CY14E064L continues SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM READ operations take

place. If a WRITE is in progress when  $\overline{\text{HSB}}$  is pulled LOW, it allows a time,  $t_{\text{DELAY}}$  to complete. However, any SRAM WRITE cycles requested after  $\overline{\text{HSB}}$  goes LOW are inhibited until  $\overline{\text{HSB}}$  returns HIGH.

The  $\overline{\text{HSB}}$  pin is used to synchronize multiple CY14E064L while using a single larger capacitor. To operate in this mode, the  $\overline{\text{HSB}}$  pin is connected together to the  $\overline{\text{HSB}}$  pins from the other CY14E064L. An external pull up resistor to +5V is required, since  $\overline{\text{HSB}}$  acts as an open drain pull down. The  $V_{CAP}$  pins from the other CY14E064L parts are tied together and share a single capacitor. The capacitor size is scaled by the number of devices connected to it. When any one of the CY14E064L detects a power loss and asserts  $\overline{\text{HSB}}$ , the common  $\overline{\text{HSB}}$  pin causes all parts to request a STORE cycle. (A STORE takes place in those CY14E064L that are written since the last nonvolatile cycle.)

During any STORE operation, regardless of how it is initiated, the CY14E064L continues to drive the  $\overline{\text{HSB}}$  pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the CY14E064L remains disabled until the  $\overline{\text{HSB}}$  pin returns HIGH.

If  $\overline{\text{HSB}}$  is not used, it is left unconnected.

### Hardware RECALL (Power Up)

During power up or after any low power condition ( $V_{CC} < V_{\text{SWITCH}}$ ), an internal RECALL request is latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{\text{SWITCH}}$ , a RECALL cycle is automatically initiated and takes  $t_{\text{HRECALL}}$  to complete.

If the CY14E064L is in a WRITE state at the end of power up RECALL, the SRAM data is corrupted. To help avoid this situation, a 10 Kohm resistor is connected either between WE and system  $V_{CC}$  or between CE and system  $V_{CC}$ .

### Software STORE

Using a software address sequence, transfer the data from the SRAM to the nonvolatile memory. The CY14E064L software STORE cycle is initiated by executing sequential CE controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0F, Initiate STORE cycle

The software sequence is clocked with  $\overline{\text{CE}}$  controlled READs or  $\overline{\text{OE}}$  controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

WRITE cycles are used in the sequence. It is not necessary that OE is LOW for a valid sequence. After the  $t_{STORE}$  cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

### Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled READ operations is performed:

1. Read address 0x0000, Valid READ
2. Read address 0x1555, Valid READ
3. Read address 0x0AAA, Valid READ
4. Read address 0x1FFF, Valid READ
5. Read address 0x10F0, Valid READ
6. Read address 0x0F0E, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and then the nonvolatile information is transferred into the SRAM cells. After the  $t_{RECALL}$  cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements.

### Data Protection

The CY14E064L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when  $V_{CC}$  is less than  $V_{SWITCH}$ . If the CY14E064L is in a WRITE mode (both CE and WE are low) at power up after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power up or brown out conditions.

### Noise Considerations

The CY14E064L is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1  $\mu$ F connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

### Low Average Active Power

CMOS technology provides the CY14E064L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 3 shows the relationship between  $I_{CC}$  and READ or WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{CC} = 5.5V$ , 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14E064L depends on the following items:

1. The duty cycle of chip enable
2. The overall cycle rate for accesses
3. The ratio of READs to WRITEs
4. CMOS versus TTL input levels
5. The operating temperature
6. The  $V_{CC}$  level
7. IO loading

Figure 3. Current Versus Cycle Time (READ)

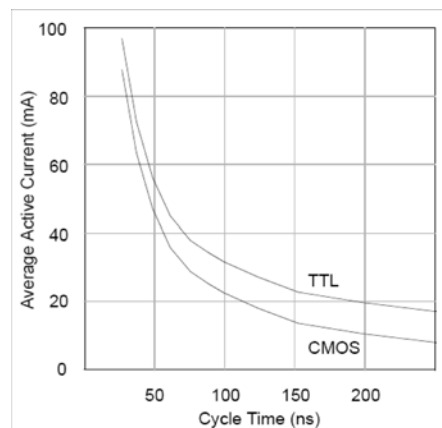
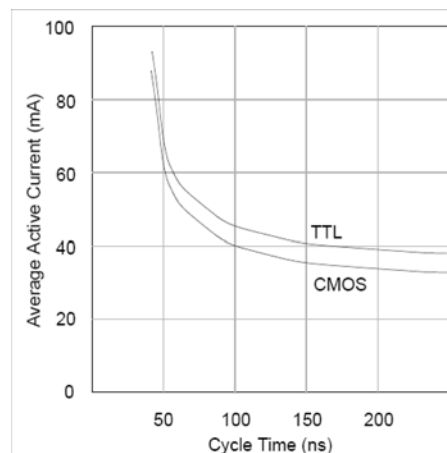


Figure 4. Current Versus Cycle Time (WRITE)



NOT RECOMMENDED FOR NEW DESIGNS  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

## Preventing STORES

The STORE function is disabled by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30 mA at a  $V_{\text{OH}}$  of at least 2.2V, because it has to overpower the internal pull down device. This device drives HSB LOW for 20  $\mu\text{s}$  at the onset of a STORE.

When the CY14E064L is connected for AutoStore operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CC}}$  and a 68  $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the CY14E064L attempts to pull HSB LOW. If HSB does not actually get below  $V_{\text{IL}}$ , the part stops trying to pull HSB LOW and abort the STORE attempt.

**Table 1. Hardware Mode Selection**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{HSB}}$	A12–A0	Mode	IO	Power
H	X	H	X	Not Selected	Output High Z	Standby
L	H	H	X	Read SRAM	Output Data	Active
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High Z	$I_{\text{CC2}}$
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0F	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $I_{\text{CC2}}$
L	H	H	0000 1555 0AAA 1FFF 10F0 0F0E	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active

**NOT RECOMMENDED FOR NEW DESIGNS**  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

### Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> Relative to GND ..... -0.5V to 7.0V

Voltage Applied to Outputs in High Z State ..... -0.5V to V<sub>CC</sub> + 0.5V

Input Voltage.....-0.5V to V<sub>CC</sub>+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -2.0V to V<sub>CC</sub> + 2.0V

Package Power Dissipation Capability (T<sub>A</sub> = 25°C) ..... 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) ..... +260°C

Output Short Circuit Current <sup>[1]</sup> ..... 15 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	4.5V to 5.5V

### DC Electrical Characteristics

Over the operating range (V<sub>CC</sub> = 4.5V to 5.5V) <sup>[2]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>CC1</sub>	Average V <sub>CC</sub> Current	t <sub>RC</sub> = 25 ns t <sub>RC</sub> = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I <sub>OUT</sub> = 0 mA.	Commercial	85 65	mA mA
I <sub>CC2</sub>	Average V <sub>CC</sub> Current during STORE	All Inputs Do Not Care, V <sub>CC</sub> = Max Average current for duration t <sub>STORE</sub>		3	mA
I <sub>CC3</sub>	Average V <sub>CC</sub> Current at t <sub>AVAV</sub> = 200 ns, 5V, 25°C Typical	$\overline{WE} > (V_{CC} - 0.2)$ . All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.		10	mA
I <sub>CC4</sub>	Average V <sub>CAP</sub> Current during AutoStore Cycle	All Inputs Do Not Care, V <sub>CC</sub> = Max Average current for duration t <sub>STORE</sub>		2	mA
I <sub>SB</sub>	V <sub>CC</sub> Standby Current	$\overline{CE} > (V_{CC} - 0.2)$ . All others V <sub>IN</sub> < 0.2V or > (V <sub>CC</sub> - 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0MHz.		2.5	mA
I <sub>IX</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Off State Output Leakage Current	V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , $\overline{CE}$ or $\overline{OE} > V_{IH}$	-5	+5	μA
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OUT</sub> = -2 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OUT</sub> = 4 mA		0.4	V

#### Notes

1. Outputs shorted for no more than one second. No more than one output shorted at a time.
2. Typical conditions for the active current shown on the front page of the data sheet are average values at 25°C (room temperature) and V<sub>CC</sub> = 5V. Not 100% tested.

### Capacitance

These parameters are guaranteed but not tested.

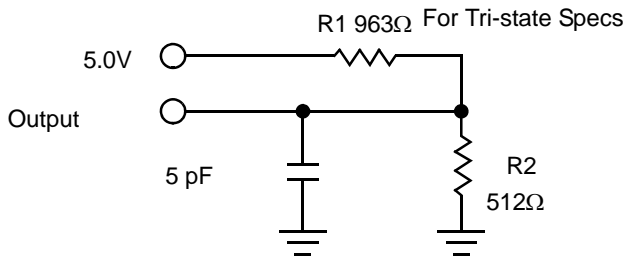
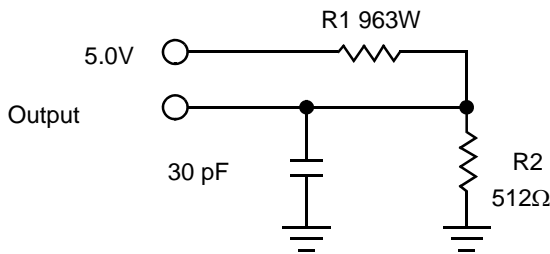
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 0 to 3.0 V	8	pF
C <sub>OUT</sub>	Output Capacitance		7	pF

### Thermal Resistance

These parameters are guaranteed but not tested.

Parameter	Description	Test Conditions	28-SOIC	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		TBD	°C/W

### AC Test Loads



### AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V  
 Input Rise and Fall Times (10% - 90%) ..... ≤5 ns  
 Input and Output Timing Reference Levels ..... 1.5 V

NOT RECOMMENDED FOR NEW DESIGNS  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE



## AC Switching Characteristics

Parameter		Description	25 ns Part		45 ns Part		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	
<b>SRAM Read Cycle</b>							
t <sub>ACE</sub>	t <sub>ACS</sub>	Chip Enable Access Time		25		45	ns
t <sub>RC</sub> <sup>[4]</sup>	t <sub>RC</sub>	Read Cycle Time	25		45		ns
t <sub>AA</sub> <sup>[5]</sup>	t <sub>AA</sub>	Address Access Time		25		45	ns
t <sub>DOE</sub>	t <sub>OE</sub>	Output Enable to Data Valid		10		20	ns
t <sub>OHA</sub> <sup>[5]</sup>	t <sub>OH</sub>	Output Hold After Address Change	5		5		ns
t <sub>LZCE</sub> <sup>[6]</sup>	t <sub>LZ</sub>	Chip Enable to Output Active	5		5		ns
t <sub>HZCE</sub> <sup>[6]</sup>	t <sub>HZ</sub>	Chip Disable to Output Inactive		10		12	ns
t <sub>LZOE</sub> <sup>[6]</sup>	t <sub>OLZ</sub>	Output Enable to Output Active	0		0		ns
t <sub>HZOE</sub> <sup>[6]</sup>	t <sub>OHZ</sub>	Output Disable to Output Inactive		10		12	ns
t <sub>PU</sub> <sup>[3]</sup>	t <sub>PA</sub>	Chip Enable to Power Active	0		0		ns
t <sub>PD</sub> <sup>[3]</sup>	t <sub>PS</sub>	Chip Disable to Power Standby		25		45	ns
<b>SRAM Write Cycle</b>							
t <sub>WC</sub>	t <sub>WC</sub>	Write Cycle Time	25		45		ns
t <sub>PWE</sub>	t <sub>WP</sub>	Write Pulse Width	20		30		ns
t <sub>SCE</sub>	t <sub>CW</sub>	Chip Enable To End of Write	20		30		ns
t <sub>SD</sub>	t <sub>DW</sub>	Data Setup to End of Write	10		15		ns
t <sub>HD</sub>	t <sub>DH</sub>	Data Hold After End of Write	0		0		ns
t <sub>AW</sub>	t <sub>AW</sub>	Address Setup to End of Write	20		30		ns
t <sub>SA</sub>	t <sub>AS</sub>	Address Setup to Start of Write	0		0		ns
t <sub>HA</sub>	t <sub>WR</sub>	Address Hold After End of Write	0		0		ns
t <sub>HZWE</sub> <sup>[6,7]</sup>	t <sub>WZ</sub>	Write Enable to Output Disable		10		14	ns
t <sub>LZWE</sub> <sup>[6]</sup>	t <sub>OW</sub>	Output Active After End of Write	5		5		ns

## AutoStore or Power Up RECALL

Parameter	Description	CY14E064L		Unit
		Min	Max	
t <sub>HRECALL</sub> <sup>[8]</sup>	Power up RECALL Duration		550	μs
t <sub>STORE</sub> <sup>[9]</sup>	STORE Cycle Duration		10	ms
V <sub>SWITCH</sub>	Low Voltage Trigger Level	4.0	4.5	V
t <sub>VCCRISE</sub>	V <sub>CC</sub> Rise Time	150		μs

### Notes

- These parameters are guaranteed but not tested.
- WE must be HIGH during SRAM Read Cycles.
- Device is continuously selected with CE and OE both Low.
- Measured ±200 mV from steady state output voltage.
- If WE is Low when CE goes Low, the outputs remain in the high impedance state.
- t<sub>HRECALL</sub> starts from the time V<sub>CC</sub> rises above V<sub>SWITCH</sub>.
- If an SRAM Write does not take place since the last nonvolatile cycle, no STORE takes place.

### Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [10,11]

Parameter	Description	25 ns Part		45 ns Part		Unit
		Min	Max	Min	Max	
t <sub>RC</sub>	STORE/RECALL Initiation Cycle Time	25		45		ns
t <sub>AS</sub>	Address Setup Time	0		0		ns
t <sub>CW</sub>	Clock Pulse Width	20		30		ns
t <sub>GLAX</sub>	Address Hold Time	20		20		ns
t <sub>RECALL</sub>	RECALL Duration		20		20	μs

### Hardware STORE Cycle

Parameter	Description	CY14E064L		Unit
		Min	Max	
t <sub>STORE</sub> [6]	STORE Cycle Duration		10	ms
t <sub>DELAY</sub> [12]	Time Allowed to Complete SRAM Cycle	1		μs
t <sub>RESTORE</sub> [13]	Hardware STORE High to Inhibit Off		700	ns
t <sub>HLHX</sub>	Hardware STORE Pulse Width	15		ns
t <sub>HLBL</sub>	Hardware STORE Low to STORE Busy		300	ns

**Notes**

- 10. The software sequence is clocked with  $\overline{CE}$  controlled READs.
- 11. The six consecutive addresses must be read in the order listed in the Mode Selection table.  $\overline{WE}$  must be HIGH during all six consecutive cycles.
- 12. Read and Write cycles in progress before  $\overline{HSB}$  are given this amount of time to complete.
- 13. t<sub>RESTORE</sub> is only applicable after t<sub>STORE</sub> is complete.

NOT RECOMMENDED FOR NEW DESIGNS  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

### Switching Waveforms

Figure 5. SRAM Read Cycle 1: Address Controlled [4, 5, 14]

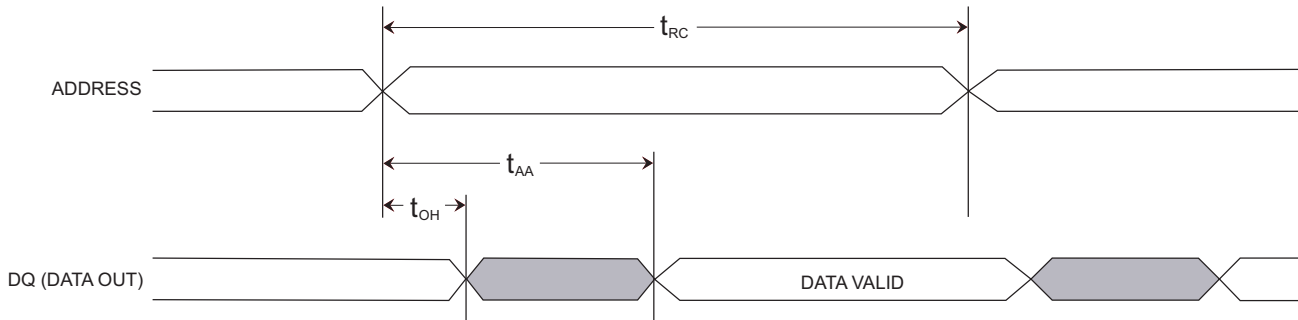
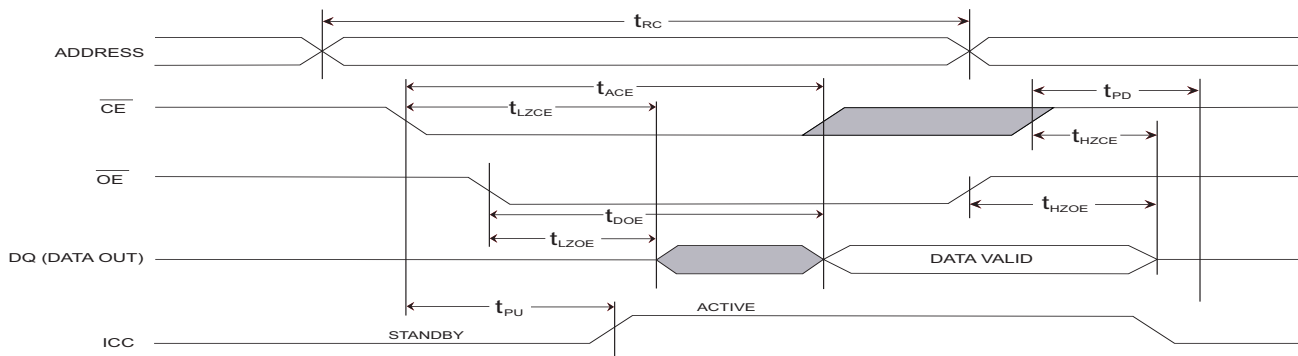


Figure 6. SRAM Read Cycle 2:  $\overline{CE}$  Controlled [4,14]



**Note**  
14. HSB must remain HIGH during READ and WRITE cycles.

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

Switching Waveforms (continued)

Figure 7. SRAM Write Cycle 1:  $\overline{WE}$  Controlled [14,15]

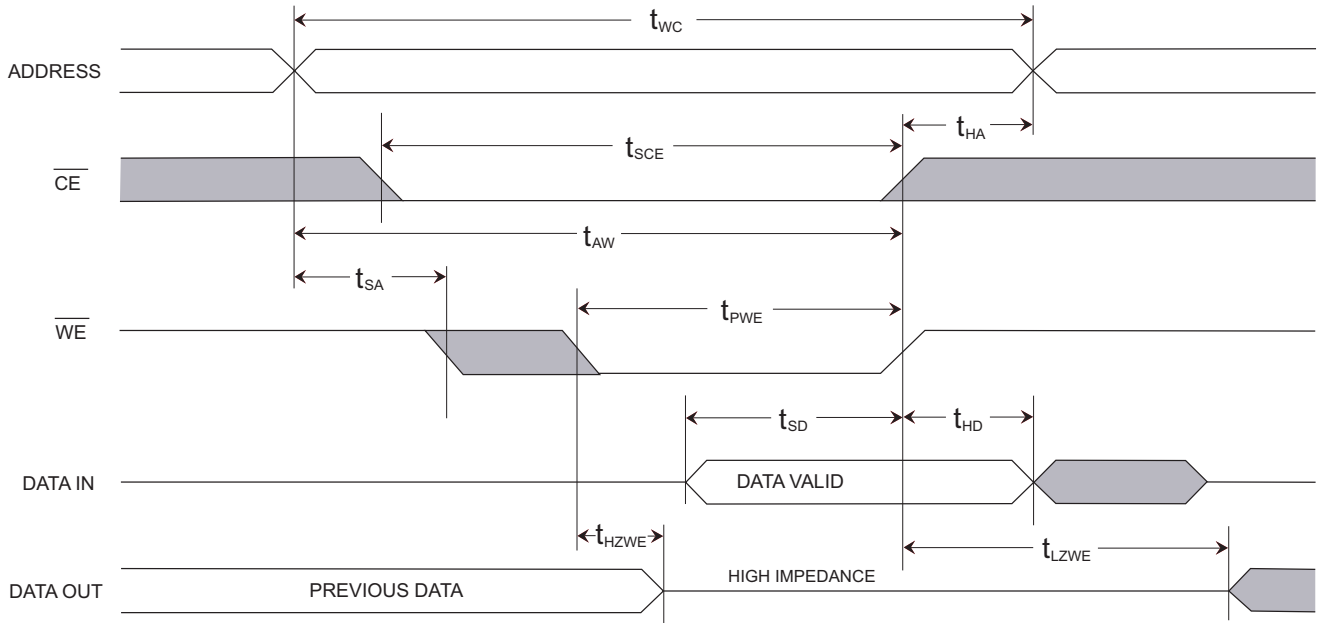
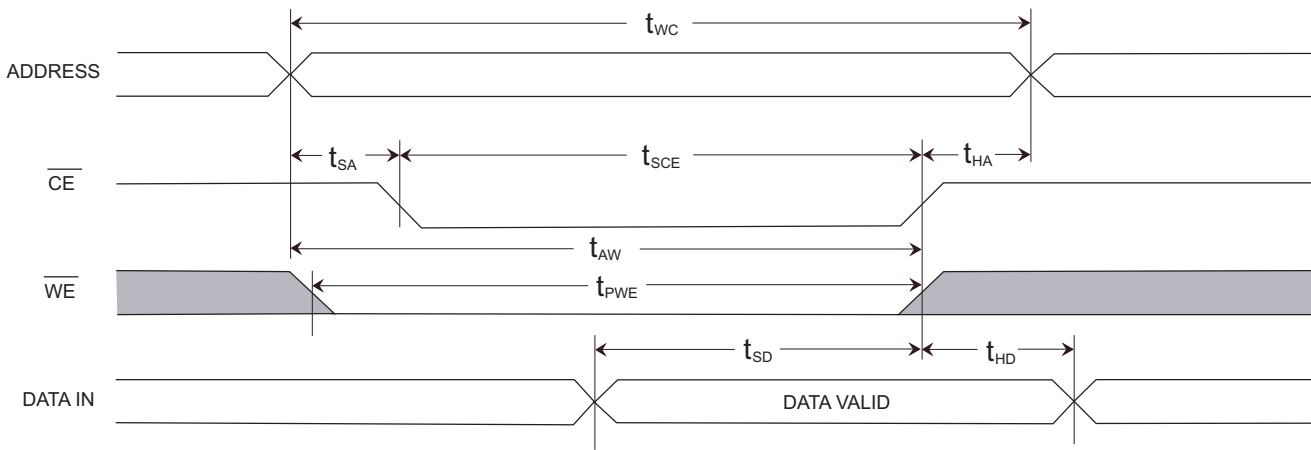


Figure 8. SRAM Write Cycle 2:  $\overline{CE}$  Controlled



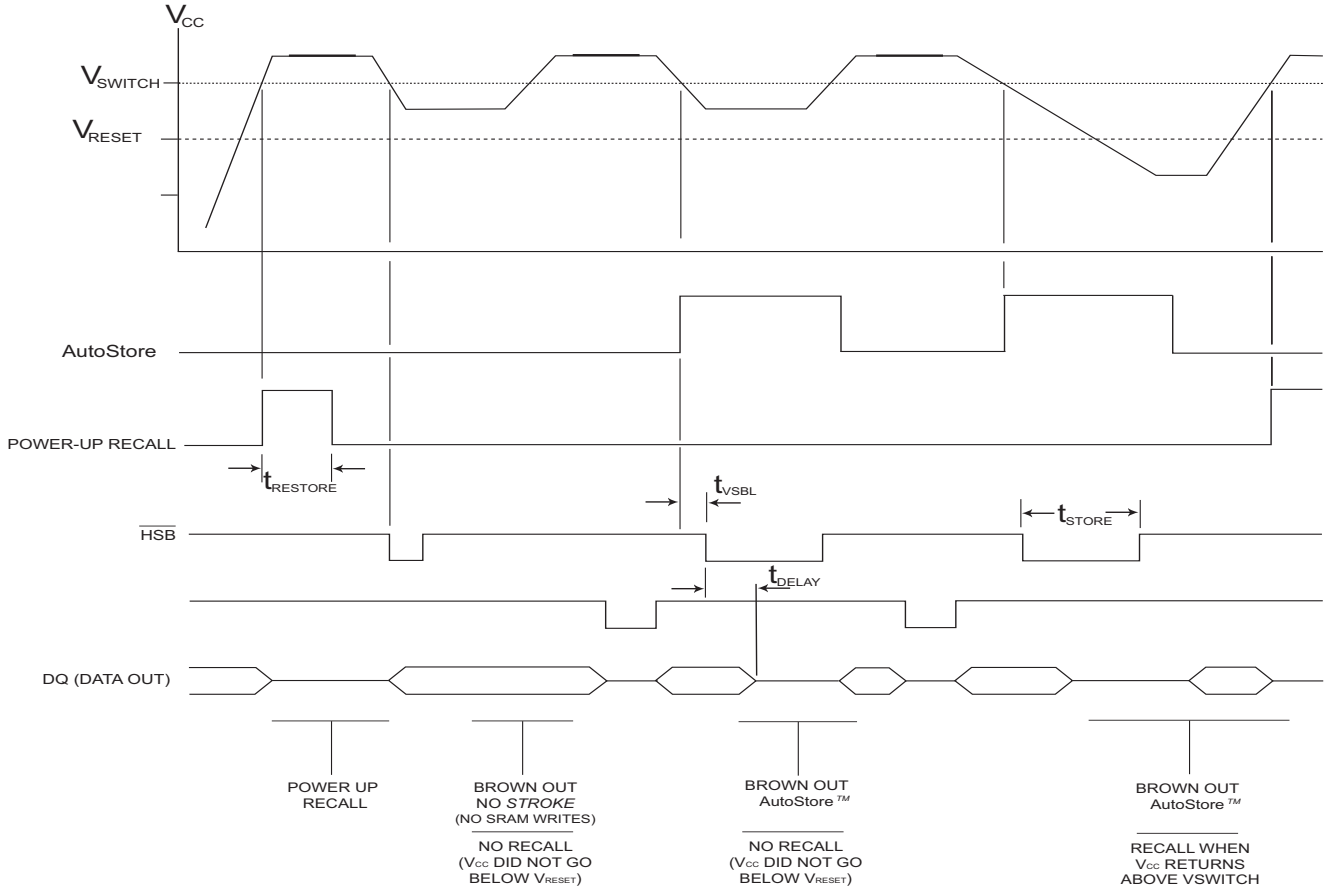
Note

15.  $\overline{CE}$  or  $\overline{WE}$  must be greater than  $V_{IH}$  during address transitions.

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

Switching Waveforms (continued)

Figure 9. AutoStore/Power Up RECALL



NOT RECOMMENDED FOR NEW DESIGNS. ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE.

Switching Waveforms (continued)

Figure 10.  $\overline{\text{CE}}$  Controlled Software STORE/RECALL Cycle <sup>[9]</sup>

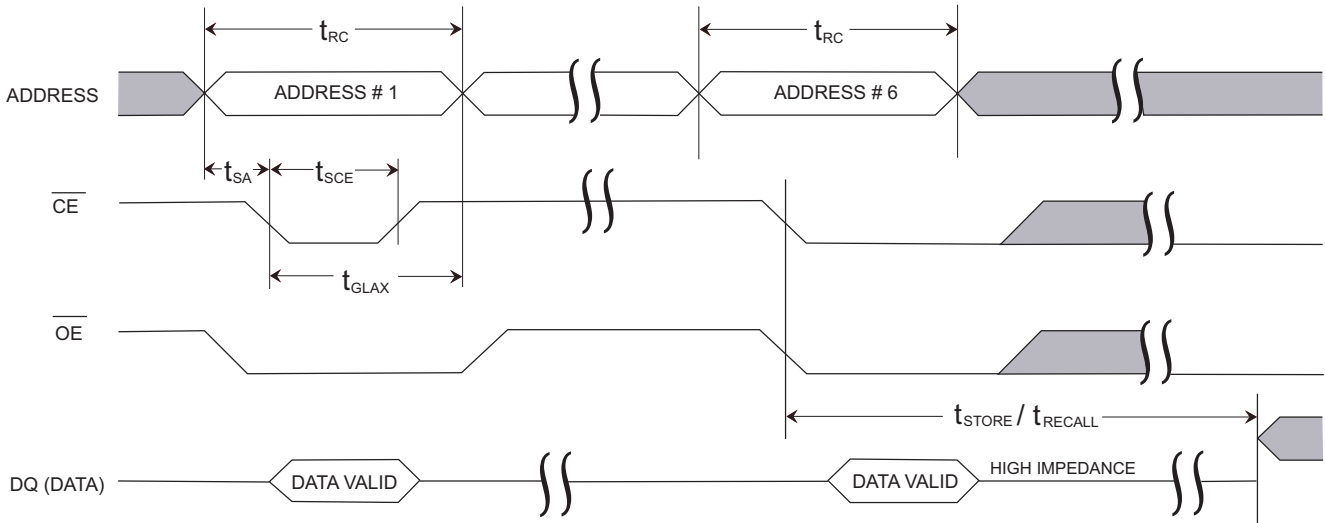
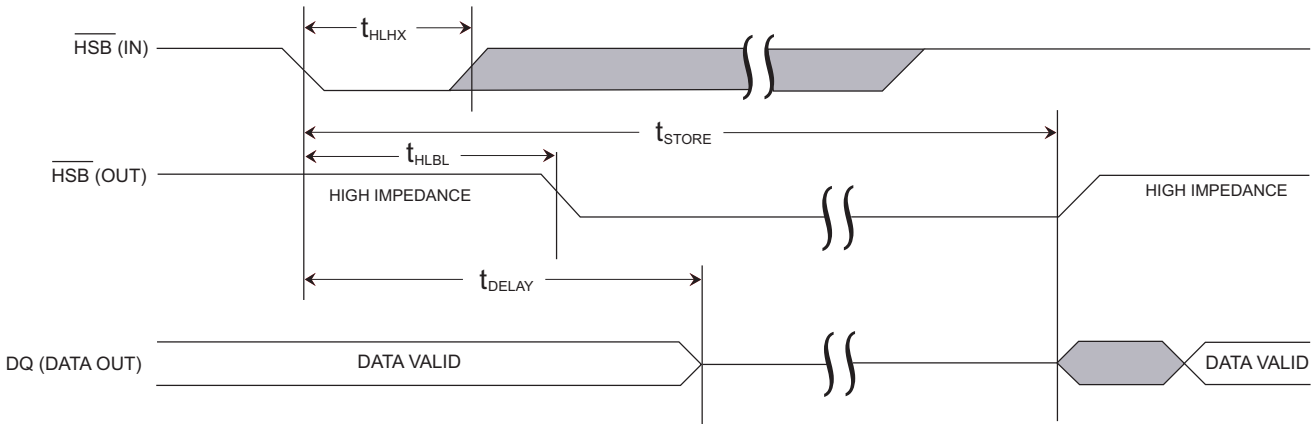


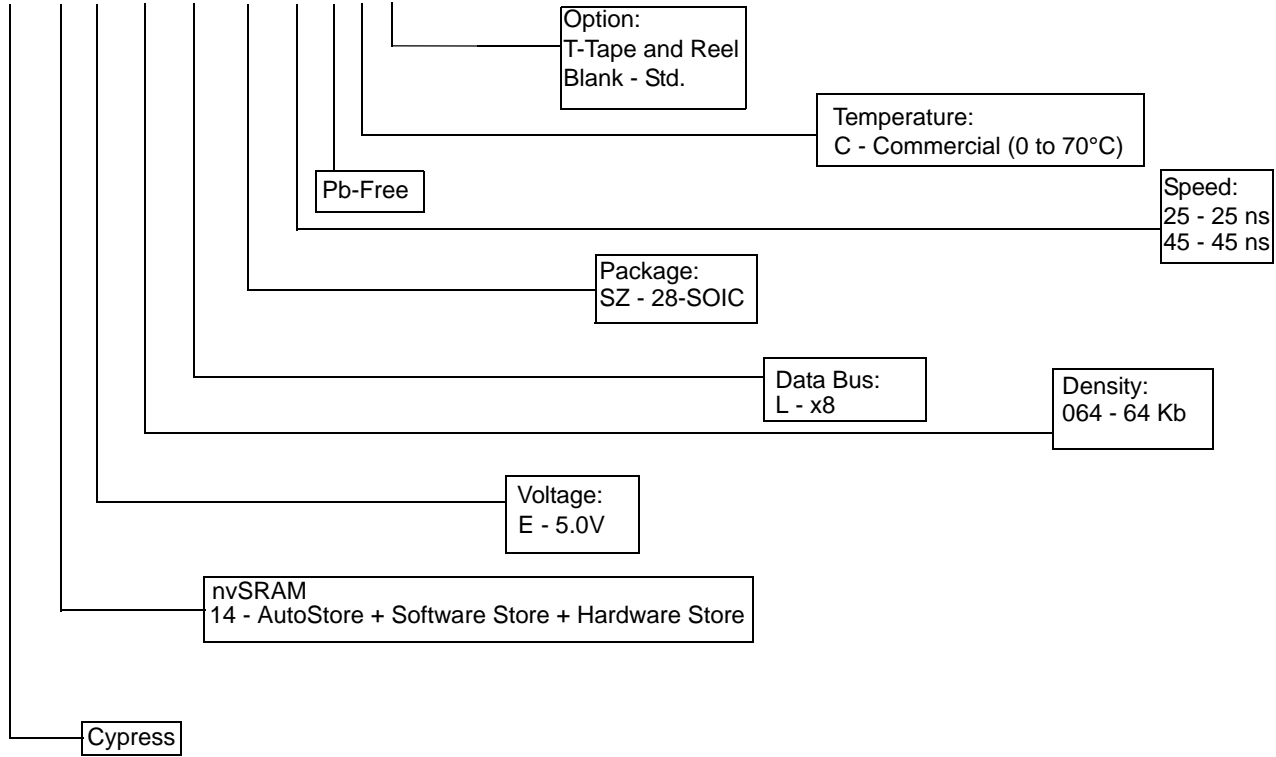
Figure 11. Hardware STORE Cycle



NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Part Numbering Nomenclature**

**CY 14 E 064 L- SZ 25 X C T**



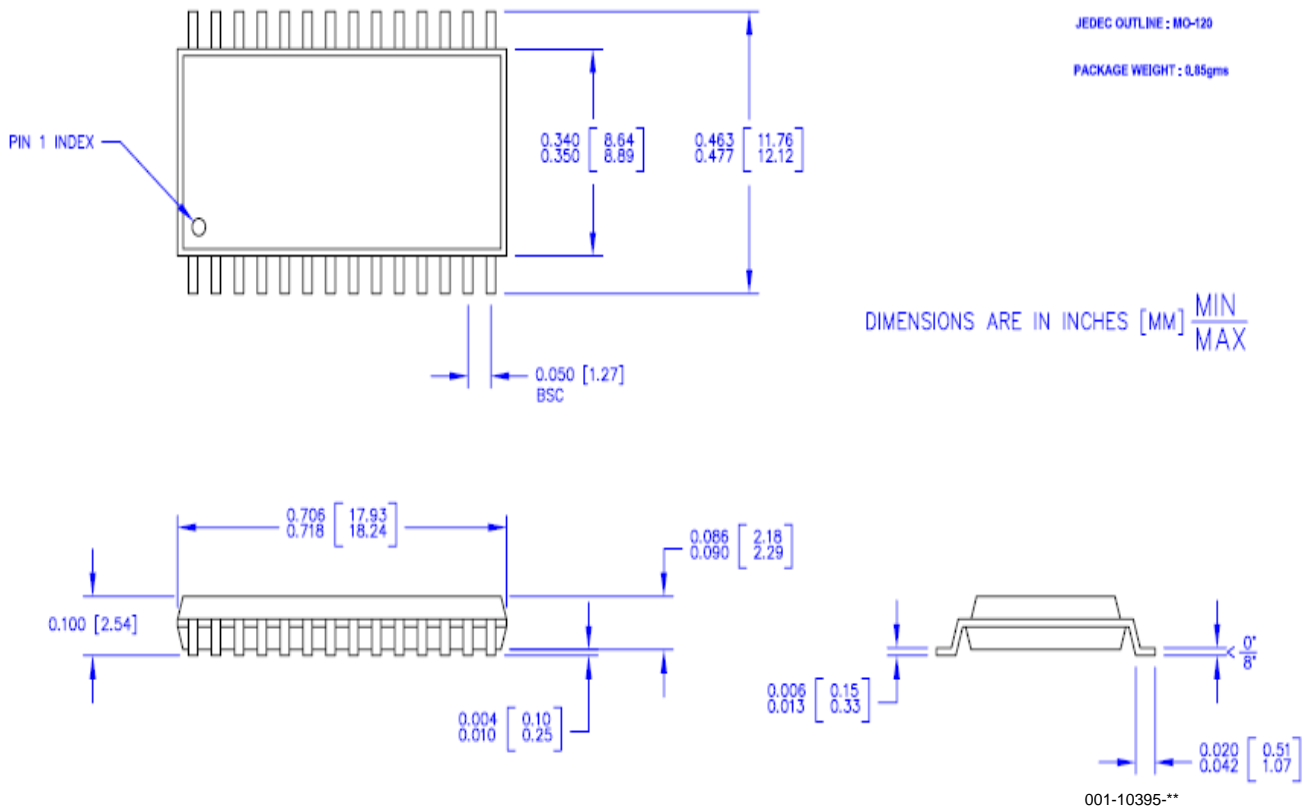
NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14E064L-SZ25XCT	001-10395	28-pin SOIC (Pb-Free)	Commercial
	CY14E064L-SZ25XC	001-10395	28-pin SOIC (Pb-Free)	
25	CY14E064L-SZ25XIT	001-10395	28-pin SOIC (Pb-Free)	Industrial
	CY14E064L-SZ25XI	001-10395	28-pin SOIC (Pb-Free)	
35	CY14E064L-SZ35XCT	001-10395	28-pin SOIC (Pb-Free)	Commercial
	CY14E064L-SZ35XC	001-10395	28-pin SOIC (Pb-Free)	
35	CY14E064L-SZ35XIT	001-10395	28-pin SOIC (Pb-Free)	Industrial
	CY14E064L-SZ35XI	001-10395	28-pin SOIC (Pb-Free)	
45	CY14E064L-SZ45XCT	001-10395	28-pin SOIC (Pb-Free)	Commercial
	CY14E064L-SZ45XC	001-10395	28-pin SOIC (Pb-Free)	
45	CY14E064L-SZ45XIT	001-10395	28-pin SOIC (Pb-Free)	Industrial
	CY14E064L-SZ45XI	001-10395	28-pin SOIC (Pb-Free)	

Package Diagrams

28-Pin (350 Mil) SOIC(001-10395)



NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE



Document History Page

Document Title: CY14E064L 64 Kbit (8K x 8) nvSRAM Document Number: 001-06543				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	427789	See ECN	TUP	New data sheet
*A	437321	See ECN	TUP	Show data sheet on Web
*B	472053	See ECN	TUP	Removed 55 ns Speed Option Updated Part Numbering Nomenclature and Ordering Information
*C	503290	See ECN	PCI	Changed from Advance to Preliminary Changed the term "Unlimited" to "Infinite" Removed Industrial Grade mention Removed 35 ns speed bin Removed Icc1 values from the DC table for 35 ns Industrial Grade Corrected V <sub>IL</sub> min specification from (V <sub>CC</sub> - 0.5) to (V <sub>SS</sub> - 0.5) Removed all references pertaining to OE controlled Software STORE and RECALL operation Included Package Diagram for 28-pin (350 mil) SOIC Updated "Part Nomenclature Table" and "Ordering Information Table"
*D	1349963	See ECN	UHA/SFV	Changed from Preliminary to Final Updated AC Test Conditions Updated Ordering Information Table
*E	2427986	See ECN	GVCH	Move to external web

© Cypress Semiconductor Corporation, 2006-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE